Monolithic Metal Oxide Transistors

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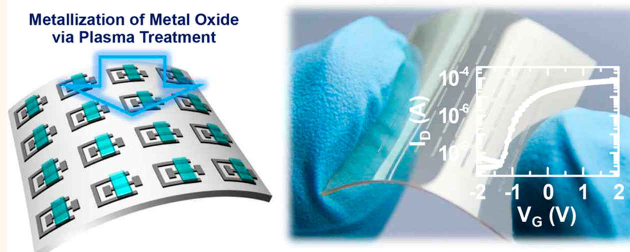
ABSTRACT We devised a simple transparent metal oxide thin film transistor architecture composed of only two component materials, an amorphous metal oxide and ion gel gate dielectric, which could be entirely assembled using room-temperature processes on a plastic substrate. The geometry cleverly takes advantage of the unique characteristics of the two components. An oxide layer is metallized upon exposure to plasma, leading to the formation of a monolithic source—channel—drain oxide layer, and the ion gel gate dielectric is used to gate the transistor channel effectively at low voltages through a coplanar gate. We confirmed that the method is generally applicable to a variety of sol—gel-processed amorphous metal oxides, including indium oxide, indium zinc oxide, and indium gallium zinc oxide. An inverter NOT logic device was assembled using the resulting devices as a proof of concept demonstration of the applicability of the devices to logic circuits. The favorable characteristics of these devices, including (i) the simplicity of the device structure with only two components, (ii) the benign fabrication processes at room temperature, (iii) the low-voltage operation under 2 V, and (iv) the excellent and stable electrical performances, together support the application of these devices to low-cost portable gadgets, *i.e.*, cheap electronics.



KEYWORDS: monolithic thin-film transistor · amorphous metal oxide semiconductors · plasma-induced metallization · cheap electronics

Flexible device technologies can create completely new markets for disposable electronics, referred to as *cheap electronics*. Cheap electronics would be realized only through simple and low-cost device fabrication processes that are done under ambient conditions. At the same time, the cheapness should not compromise the resulting device performance and stability. Solution processing of a variety of semiconductors, including organic molecules,[1−7] polymers,[8−11] carbon nanomaterials,[12−17] and colloidal nanomaterials,[18,19] has been developed intensively over the last few decades. The resulting devices, however, often yield performances and operational stabilities that are inferior compared to the corresponding properties of devices prepared using vacuum-processed semiconductors. Alternatively, sol—gel-processed amorphous metal oxide semiconductors (AOS) show promise for the realization of cheap electronics because both the performance and stability properties of the resulting devices remain high.[20−32] In addition, the amorphous film yields devices that display reliable reproducible performances over a large integrated area. Moreover, the high optical transparency and good mechanical flexibility of the materials provide additional functionalities to these devices.[25,29,33] Sol—gel-processed AOS devices do, however, suffer from a critical drawback in that sol—gel processes typically require a high annealing temperature to induce the sol—gel reaction; thin films annealed at higher temperatures yield higher conductivities.[20,23,26,27] Unfortunately, this high temperature requirement prohibits the use of the materials with flexible cheap substrates, such as plastic or paper.

Additionally, the inherent complexity of conventional electronic device structures containing multiple functional components can increase the device cost by requiring multiple fabrication steps. For instance, thin film transistors (TFTs), which are a basic functional unit of electronics, require at least three functional elements: the thin film semiconductor channel, the gate dielectric, and the electrodes.[3] These three elements

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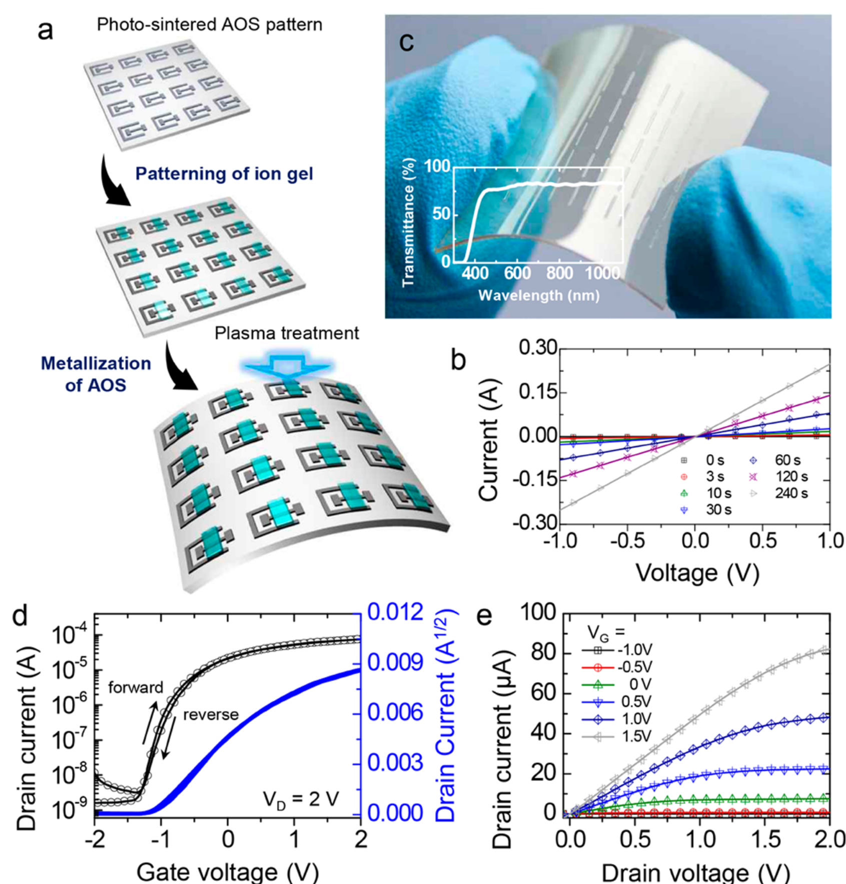

Figure 1. Device fabrication and characterization. (a) Schematic diagram of the monolithic metal oxide transistor fabrication process on a plastic substrate. (b) Current−voltage characteristics of an In_2O_3 film exposed to Ar plasma for different periods, with increasing Ar plasma treatment of time. (c) Photographic image of the monolithic In_2O_3 transistor array. The inset shows the optical transmittance of the transistor array. Output (d) and transfer (e) characteristics of a monolithic In_2O_3 transistor.

are typically formed from three different component materials that require three different processing steps. Although previous efforts have mainly concentrated on the development of new materials and processing methods, even more significant reductions in the device fabrication costs may be achieved by devising an innovative device geometry that allows one to assemble devices in a simpler manner.

To address these issues, we developed a very simple route to fabricating AOS TFTs on plastic substrates through a room-temperature fabrication process.[29] An unconventional transistor structure was devised to allow fabrication of the entire device using only two functional materials: AOS and an electrolyte. The resulting transistors based on amorphous indium oxide (In_2O_3) yielded an electron mobility as high as 6.7 $cm^2/V \cdot s$ under sub-2 V operation. The device also demonstrated a sustained operational stability during bending experiments under ambient conditions. The method could be successfully applied to other AOSs, such as indium−zinc oxide (IZO) or indium−gallium−zinc oxide (IGZO). The proof-of-concept assembly of a basic NOT-logic circuit was demonstrated using the as-prepared In_2O_3 TFTs. The simple fabrication processes presented here yielded both an excellent device performance and a good reliability. We believe that these devices have achieved a critical milestone on the path toward realizing cheap flexible electronics.

RESULTS AND DISCUSSION

The simple In_2O_3 TFT fabrication processes are illustrated in Figure 1a. First, an In_2O_3 layer was formed through a photochemically driven sol−gel process at room temperature on a plastic substrate.[29] This layer was formed by applying an Al_2O_3 precoating on a plastic substrate to create a hydrophilic surface that was appropriate for subsequent application of the polar In_2O_3 precursor solution composed of indium nitrate hydrate dissolved in 2-methoxyethanol. After the precursor solution was spin-coated onto the Al_2O_3 coated substrate, the film was dried at 60 °C and then irradiated with deep-UV (wavelength = 253.7 and 184.9 nm) to form an In_2O_3 metal−oxygen−metal network film. Subsequently, the photochemically activated films were patterned using conventional photolithography and etching processes. The patterning process produced patches of a U-shaped In_2O_3 layer surrounding a hammer-shaped In_2O_3 layer, which served, respectively, as the coplanar gate and monolithic

source-channel drain of a TFT after the plasma activation process described below.[34] A highly capacitive ion gel gate dielectric (specific capacitance = 2.2 μF/cm^2) based on a poly(ethylene glycol) diacrylate (PEGDA) prepolymer, 2-hydroxy-2-methylpropiophenone (HOMPP) photoinitiator, and 1-ethyl-3-methylimidazolium bis(trifluoromethanesulfonyl)imide ([EMIM][TFSI]) ionic liquid was partially applied onto the In_2O_3 patches. The ion gel layer formed bridges between the U-shaped and the hammer-shaped patches of the In_2O_3 layer during UV patterning through a photomask. Subsequently, Ar plasma (200 W) was applied to the substrate to induce metallization of the In_2O_3 layers[35,36] that were directly exposed to the plasma. X-ray photoelectron spectroscopy (XPS) analysis (Figure S1, Supporting Information) revealed that the exposure of the In_2O_3 layers to a plasma produced oxygen vacancy sites, which dramatically reduced the resistivity after 4 min of exposure, as shown in the evolution of current−voltage curves (Figure 1b) and transfer curves (Figure S2, Supporting Information). During this process, the patterned ion gel layer played an additional role of as a protection layer for the underlying In_2O_3 layer. The protection layer prevented direct exposure of In_2O_3 to Ar plasma, which would have metallized the In_2O_3. Consequently, a monolithic hammer-shaped In_2O_3 patch partially covered with the ion gel layer could be functionalized to produce source (metallized section), channel (protected section), and drain (metallized section) components. Similarly, the neighboring U-shaped In_2O_3 patch could be functionalized partially to produce a coplanar gate (metallized section). Figure 1c shows a photographic image of a coplanar In_2O_3 transistor array fabricated on a plastic substrate. The device array displayed an optical transparency of ~80% at 550 nm as shown in the inset.

Within this unique transistor structure, electrons accumulate and flow in the In_2O_3 channel under a positive applied bias at the coplanar gate voltage upon forming electric double layer (EDL) at the electrolyte/channel interface.[37] Because the EDL at the interface is formed as long as the electric field is applied across the gate and channel, the EDL could be formed not only in a conventional sandwich-type gating geometry but also in a coplanar gate geometry. Figure 1d shows the transfer characteristics (drain current (I_D) − gate voltage (V_G)) measured at a constant drain voltage of V_D = 2 V for a coplanar In_2O_3 transistor. The device turned on sharply near $V_G = -1$ V with a subthreshold swing of 130 mV/decade. In addition, the high capacitance of the ion gel gate dielectric (2.2 μF/cm^2) yielded high current (~0.1 mA) at low operation voltages below 2 V. Negligible current hysteresis between the forward and reverse V_G traces was observed, indicating a low interfacial trap state density at the In_2O_3/ion gel interface. The statistical distribution of performance properties obtained from 50 monolithic In_2O_3 transistors fabricated in different batches is shown in Figure S3 (Supporting Information). The histogram reveals an average electron mobility of 3.6 (±1.2) cm^2/V·s, threshold voltage (V_{th}) of −0.3 (±0.3) V, and on/off current ratio of 5.9 (±1.6) × 10^4. Note that a maximum electron mobility of 6.7 cm^2/V·s was obtained. These results are summarized in Table 1. Figure 1e shows typical output characteristics ($I_D - V_D$) of the In_2O_3 transistor under six different applied V_G's. The device exhibited reasonable gate modulations both in the linear and saturation transistor operation regimes.

TABLE 1. Summary of Electrical Properties of Monolithic In_2O_3, IZO, and IGZO Transistors Including Electron Mobility, on/off Current Ratio, and Threshold Voltage

	electron mobility (cm^2/V·s)	on/off current ratio	threshold voltage (V)
In_2O_3	3.6 (±1.2)	5.9 (±1.6) × 10^4	−0.3 (±0.3)
IZO	1.3 (±0.2)	6.5 (±1.8) × 10^4	−0.1 (±0.2)
IGZO	1.6 (±0.3)	7.1 (±1.4) × 10^4	0.0 (±0.2)

We noticed that the carrier mobility of these devices was higher than that obtained from conventional SiO_2-gated field-effect devices (Figure S4, Supporting Information). Typically, higher carrier mobilities were obtained from an AOS system that was gated using an electrolyte gate dielectric, such as an ion gel, compared to the carrier mobilities obtained from conventional SiO_2 gate dielectrics.[38−40] The highly capacitive electrolyte induced a much higher charge density within the channel that filled many carrier traps near the transport level, which in turn, leads to a more efficient charge transport. In addition to this effect, the device geometry of our devices enhanced the carrier mobility. The unique monolithic nature of the source−channel−drain geometry of the as-prepared devices improved charge injection from the electrode to the semiconductor or reduced the injection resistance ($R_{injection}$) compared to the corresponding values obtained from conventional metal oxide transistors with separate source−drain metal contacts under or on top of the channel. The interfacial properties in the metallized In_2O_3/unmetallized In_2O_3 homojunction in these devices are apparently superior to those obtained in typical metal/In_2O_3 heterojunctions fabricated with separate metal contacts. Furthermore, the use of a coplanar gate device configuration, such as the configuration described in this work, created metallized source/drain regions positioned within the semiconducting channel plane (Figure 2a) because metallization by an Ar plasma occurred mainly at the top surface of the In_2O_3 layer. The access resistance (R_{access}), which represents the resistive character of the device preventing the injected charges from reaching the transport channel, was significantly reduced in our device structure.

These effects were confirmed by evaluating the lumped contact resistance (R_C) of the monolithic

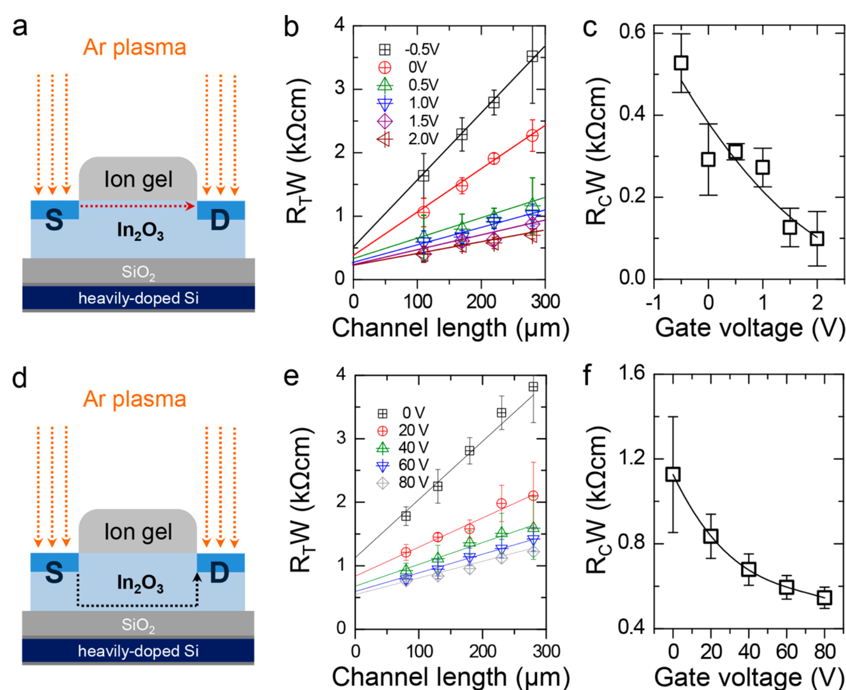

Figure 2. Charge injection in the monolithic In_2O_3 transistor. (a) Schematic diagram of the monolithic In_2O_3 transistor operated using an ion gel by the coplanar gate. The transport channel was formed at the uppermost region of the In_2O_3 film in contact with the ion gel. (b) The channel-width-normalized total resistance (R_T) of a monolithic In_2O_3 transistor plotted as a function of the channel length at different gate voltages. (c) Channel-width-normalized contact resistance (R_C) extracted from (b), plotted as a function of the gate voltage obtained from (b). (d) Schematic diagram showing the monolithic In_2O_3 transistor operated using the bottom SiO_2/Si gate. The transport channel in this case was formed at the lowermost region of the In_2O_3 film in contact with the bottom SiO_2 gate dielectric layer. (e) Channel-width-normalized R_T for the In_2O_3 film gated through the SiO_2 dielectric layer, plotted as a function of the channel length at different gate voltages. (f) Channel width normalized R_C extracted from (e) and plotted as a function of the gate voltage.

In_2O_3 transistor, which includes both $R_{injection}$ and R_{access}, based on the channel length-dependent resistance of the devices measured using the transmission line method (TLM).[41] These measurements were collected using devices fabricated on Si/SiO_2 wafers rather than using those fabricated on PAR substrates. The channel length of the device was varied from 100 to 250 μm, while the channel width remained fixed at 1 mm. The channel width normalized total resistance of the transistors is plotted in Figure 2b as a function of the channel length for each V_G value applied to the coplanar gate. The R_C could be extracted from the *y*-intercept of the linear fit of the total resistance obtained at each V_G. Figure 2c shows the width-normalized contact resistance (R_CW) as a function of V_G. The R_CW decreased from 527 to 98 Ωcm as V_G was varied from −0.5 to 2 V. This value was substantially lower than the values measured from typical MO transistors using conventional metallic contacts[21,35] and was comparable to the homojunctioned IGZO TFTs prepared using H_2 plasma-treated source−drain contacts.[42] Additionally, the values of R_C in the same monolithic In_2O_3 transistors were measured using TLM again, but this time the gate bias was applied through the bottom Si/SiO_2 gate dielectric. Under a field applied to the bottom gate, the transport channel formed at the very bottom of the In_2O_3 layer in contact with the SiO_2 layer, and thus, different R_{access} values were expected. These results are plotted in Figure 2d,e, and the corresponding *I*−*V* characteristics of the devices are plotted in Figure S5 (Supporting Information). As the In_2O_3 layer was gated through the bottom, the value of R_CW varied from 1126 to 546 Ω cm as V_G varied from 0 to 80 V. The data obtained from the same set of devices were averaged, so the value of $R_{injection}$ under both types of gating configurations was assumed to remain constant. The offset was qualitatively attributed to the difference between R_{access} and the superior accessibility of the charges injected into the transport channel in the ion gel-gated devices.

The operational features of the metallized In_2O_3 coplanar gate and ion gel interface under an applied gate bias were explored. The operation of a gate with the given structure requires contact between the metallized gate and the electrolyte (unlike the operation of a source and drain, which operates better in the absence of contact with the electrolyte). Otherwise, EDL at the gate/electrolyte interface is hardly formed. The ion gel in our device functioned as a protective mask that prevented metallization, suggesting that the metallized gate that was formed within the unmasked In_2O_3 areas and the mask ion gel layer should, in principle, be separated from the electrolyte. In this view, the operational mechanism of the gate may seem

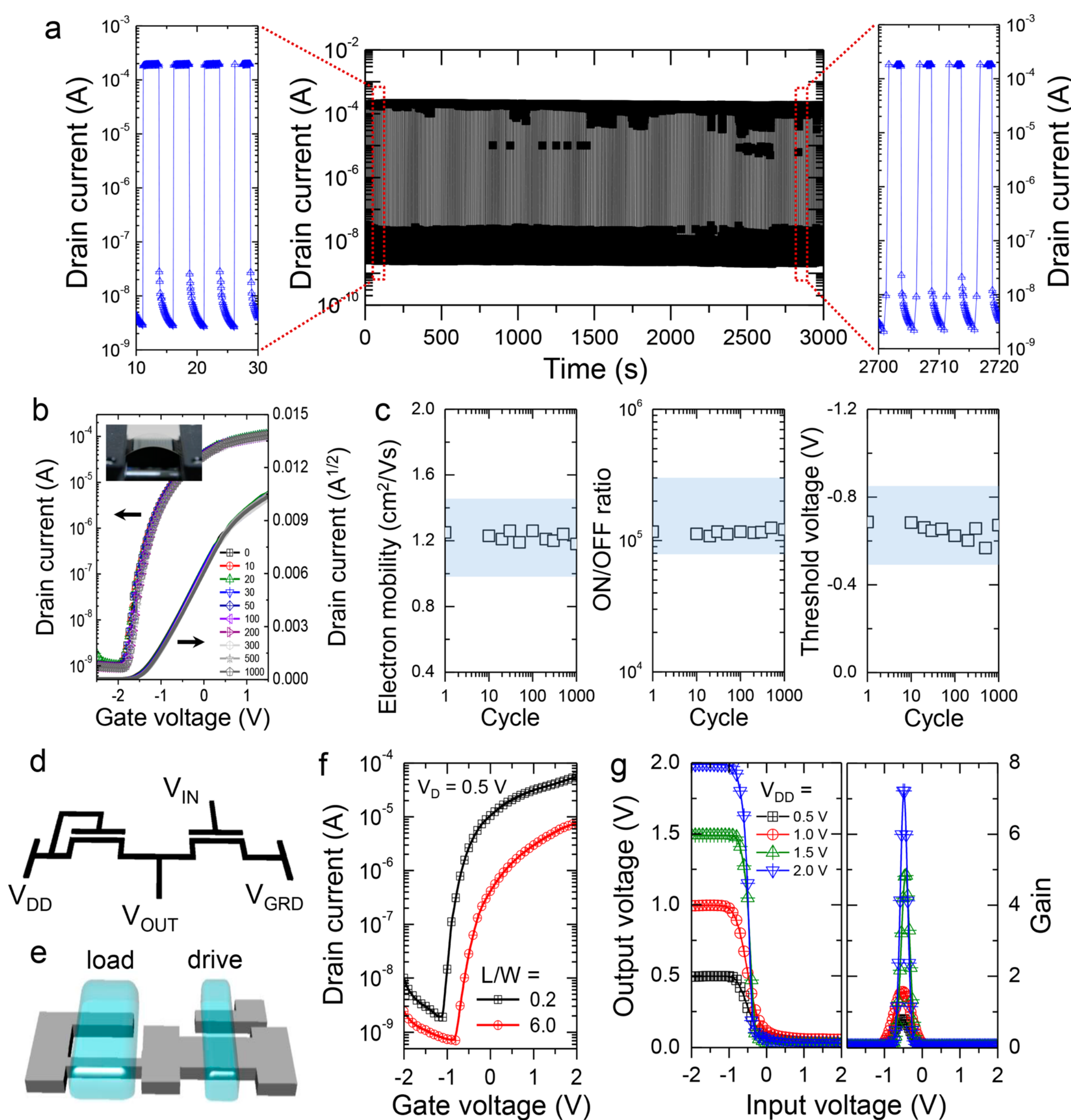

Figure 3. Operational and mechanical stabilities of the monolithic In_2O_3 transistor, and demonstration of a NOT-inverter logic circuit. (a) Evolution of the current level in a monolithic In_2O_3 transistor during continuous cycling between on (V_G = 2 V) and off (V_G = −2 V) states. (b) Evolution of the transfer characteristics of the monolithic In_2O_3 transistor during 1000 fatigue cycles (compressive strain = 0.5%). (c) Changes in the electron mobility, on/off current ratio, and threshold voltage, plotted as a function of the number of compression and release cycles. A circuit diagram (d) and a schematic diagram (e) of an inverter NOT-logic circuit based on two monolithic In_2O_3 transistors with different channel geometries (*L*/*W*). (f) Transfer characteristics of the constituent transistors: the drive transistor (*L*/*W* = 200 μm/1000 μm, black) and the load transistor (*L*/*W* = 300 μm/50 μm, red). (g) Input−output voltage characteristics of the inverter under various V_{DD}s and their corresponding gains.

counterintuitive, as direct contact between the metallized gate electrode and the ion gel layer is not present. The device operation, indeed, relies on the swelling of the protective ion gel layer upon exposure to an Ar plasma. As shown in Figure S6 (Supporting Information), the original square-patterned ion gel slowly swelled during the 4 min plasma treatment process. Taking advantage of the swelling of the protective ion gel, metallized In_2O_3 formed, even beneath the ion gel layer, especially around the original boundary of the ion gel layer prior to swelling. This boundary zone was exposed to an Ar plasma initially, but it became protected by the swollen ion gel layer upon further plasma treatment. In this manner, direct contact between the metallized gate and the electrolyte could be formed to allow gating of the current levels through the device channel. Because the contacting area of the metallized gate beneath the ion gel layer was small, the capacitance of the ion gel layer in our system was small relative to the capacitances observed in conventional EDL systems.

The realization of practical, cheap, flexible electronics requires low device fabrication costs as well as reliable performance.[26,29,32] The operational and

mechanical stabilities of the In_2O_3 transistors developed were, therefore, investigated. Changes in the transistor characteristics of the In_2O_3 devices were monitored during continuous on/off switching cycles and mechanical bending cycles. Dynamic stress tests were performed by cycling the devices continuously between on ($V_G = +2$ V) and off ($V_G = -2$ V) states while holding V_D at 2 V. Figure 3a shows the drain−current levels of the devices during the alternating V_G cycles over 1 h. The on/off current ratio of $\sim 10^5$ remained invariant, even after 500 gate voltage cycles, over a 1 h time period. Next, the mechanical stabilities of the monolithic In_2O_3 transistors were analyzed by performing cyclic bending tests over 1000 cycles. An In_2O_3 transistor device array prepared on a plastic substrate was bent (0.5% compressive strain) and relaxed repeatedly. Representative transfer curves measured from the device were collected after a given numbers of cycles, as shown in Figure 3b. No obvious failure or degradation in the operation was observed, even after 1000 bending cycles. The device characteristics, including the electron mobility, on/off current ratio, and threshold voltage of the devices, remained invariant during the bending cycles (Figure 3c). Overall, these results demonstrated that our monolithic In_2O_3 transistors exhibited stable operational and mechanical properties.

A proof-of-concept demonstration of the In_2O_3 transistor applicability to logic circuits was conducted by assembling a basic NOT-inverter logic device.[7] Two monolithic In_2O_3 transistors with different channel L/W ratios were connected in series (Figure 3d). The transfer characteristics of the two transistors are shown in Figure 3f, providing evident for differences in the current levels.[43] The transistor with a larger L/W ratio ($L = 300\ \mu$m/$W = 50\ \mu$m) served as the load while that with the smaller L/W ratio ($L = 200\ \mu$m/$W = 1000\ \mu$m) served as the drive of the inverter (Figure 3e). The logic circuit was formed by connecting the load transistor to the supply voltage (V_{DD}) and the drive transistor to the ground. The two transistors shared an output terminal. It should be emphasized that these devices were fabricated in three simple steps: formation of In_2O_3 patches, bridging the patches with ion gel layers, and subsequent Ar plasma treatment. Under a positive V_{DD} and negative V_{IN}, the load and drive transistors were present in on and off states, respectively, and thus, the V_{OUT} signal traced the V_{DD} value. As the V_{IN} applied to the drive transistor increased, the drive transistor turned on, and the channel resistance dropped below the resistance of the load transistor. This effect dramatically reduced the V_{OUT} signal, *i.e.*, the signal inverted. Figure 3g shows the successful inversion of a monolithic In_2O_3 inverter at different V_{DD}'s. As V_{DD} was varied from 0.5 to 2 V, the output voltage (V_{OUT}) remained comparable to the V_{DD} at low V_{IN}. As V_{IN} increased, V_{OUT} promptly dropped to 0 V. The signal inversion

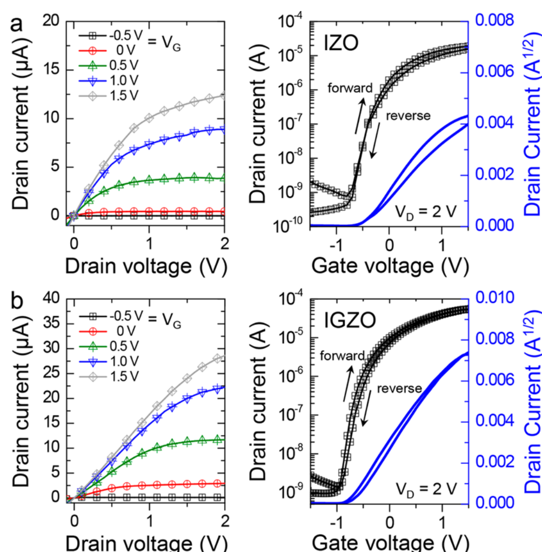

Figure 4. $I-V$ relationships in other monolithic AOS TFTs. Output and transfer characteristics of the monolithic IGZO (a) and IZO (b) TFTs.

(positioned at a negative voltage region) can be manipulated by controlling the V_{th}s of the transistors. The calculated signal inverter gain (dV_{OUT}/dV_{IN}) is displayed in the right panel. The signal inverter gain increased with V_{DD}, and the maximum gain value exceeded 7 at V_{DD} = 2 V, revealing the successful demonstration of our monolithic In_2O_3 transistors for use in simple circuit applications.

Finally, the novel strategy demonstrated here using amorphous In_2O_3 thin films was successfully applied to other sol−gel-processed AOS systems, including IZO and IGZO. The output and transfer characteristics of the IZO and IGZO transistors prepared using the procedure described above are shown in parts a and b, respectively, of Figure 4. These curves revealed transistor performances that were similar to those of the In_2O_3 devices. Table 1 summarizes the electrical properties of the different AOS TFTs, including the electron mobility, on/off ratio, and threshold voltage. These results indicated that the method presented here could be generalized for a family of AOS systems.

CONCLUSION

In conclusion, we demonstrated the fabrication and operation of monolithic metal oxide transistors composed of only two materials for the realization of electrode, channel, and gate dielectric components. These components could be prepared entirely *via* room-temperature processing on plastic substrates. The unique device structure relied on the selective metallization of an oxide layer using plasma and on the coplanar gating of the transistor channel through the ion gel gate dielectric. This geometry was successfully applied to various AOSs, including In_2O_3, IZO, and IGZO, and the resulting performances, including the carrier mobility and operational voltage, were superior

to those measured in reference devices having a conventional structure. Overall, the simple device geometry allowed fabrication of AOS TFTs without compromising the excellent electrical and mechanical performances of the components. The proposed device geometry and its unique fabrication method constitute a significant contribution toward the realization of cheap, disposable, and flexible electronics.

METHODS

Device Fabrication. A poly-4-vinylphenol (PVP) solution was first prepared by dissolving PVP (1.6 g) and poly(melamine-*co*-formaldehyde) (PMF, 0.8 g) in a propylene glycol monomethyl ether acetate (PGMEA) solvent (18.2 mL). The PVP solution was then spin-coated onto a polyarylate (PAR) flexible substrate (thickness = 200 μm) (A200HC, Ferrania Technologies) at 2000 rpm for 60 s, followed by thermal annealing at 120 °C for 12 h inside a vacuum oven to cross-link the PVP. An Al_2O_3 layer (thickness = 40 nm) was deposited onto the cross-linked PVP/PAR substrate using an atomic layer deposition process and then was treated with UV illumination under an oz1 atm for more than 600 s (λ_{peak} = 254 nm, intensity = 28 mW/cm^2). Separately, a solution of indium oxide precursor was prepared by dissolving 0.1 mol of indium nitrate hydrate (Sigma-Aldrich, 99.999%) in 10 mL of 2-methoxyethanol. The prepared solution was stirred at 75 °C for 12 h and filtered through a 0.2 μm PTFE membrane. This precursor solution was spin-coated onto the Al_2O_3 substrate at 4000 rpm for 30 s and then dried for 2 min on a hot plate (60 °C). The resulting indium oxide layer was sintered using a high-density deep-UV treatment system (UV253H, Filgen) under N_2 flow for 2 h. The resulting indium oxide was patterned through photolithography using an AZ 5214 and AZ 500 MIF developer and was subsequently wet-etched using a 4% LCE-12 solution. The gate dielectric layer was formed by drop-casting an ion-gel solution comprising poly(ethylene glycol) diacrylate (PEGDA, Sigma-Aldrich), 2-hydroxy-2-methylpropiophenone (HOMPP, Sigma-Aldrich), and 1-ethyl-3-methylimidazolium bis(trifluoromethanesulfonyl)imide ([EMIM][TFSI]) ionic liquid (Merck) in a weight ratio of 2:1:22 onto the indium oxide patterned substrate. After drying, the ion gel film was partially exposed to UV (350 W) for 10 s through a photomask. This led to the photoinduced cross-linking of PEGDA to form a gel. The unexposed region was removed by DI water and dried using an air gun. Finally, the entire substrate was exposed to an Ar plasma (200 W, 0.1 Torr) to induce metallization of the In_2O_3 layer over various treatment times.

Measurements. The optical transmittance of the transistor array was characterized using UV−vis spectrophotometry (Agilent 8453). The *I*−*V* transistor characteristics were obtained at room temperature under ambient dark conditions using Keithley 2400 equipment and 236 source/measure units.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Figures S1−S6. This material is available free of charge *via* the Internet at http://pubs.acs.org

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